FIG. 1

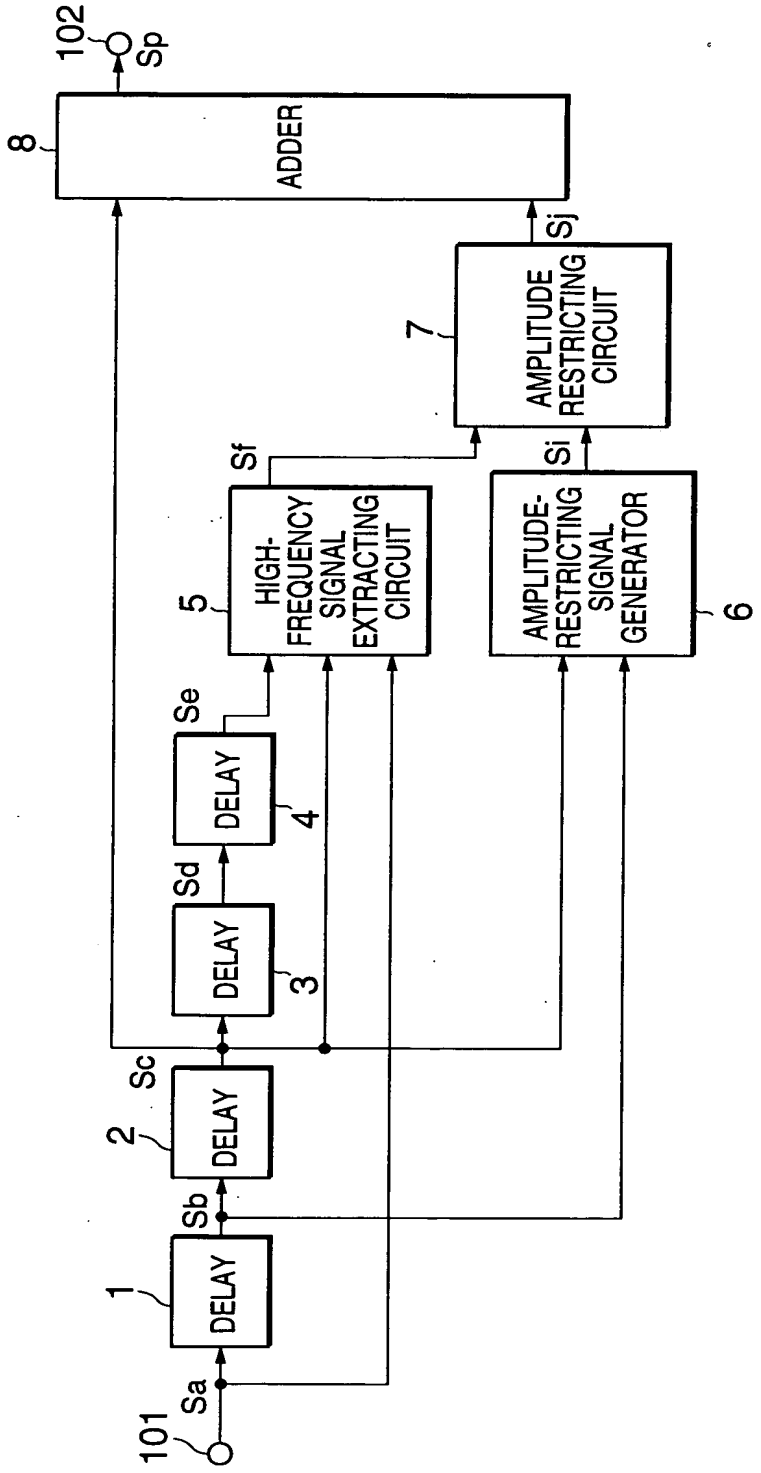
101
Sa
1
DELAY
Sb
2
DELAY
Sc
3
DELAY
Sd
4
DELAY
Se
5
HIGH-FREQUENCY SIGNAL EXTRACTING CIRCUIT
Sf
6
AMPLITUDE-RESTRICTING SIGNAL GENERATOR
Si
7
AMPLITUDE RESTRICTING CIRCUIT
Sj
8
ADDER
102
Sp

FIG. 2A
Sa

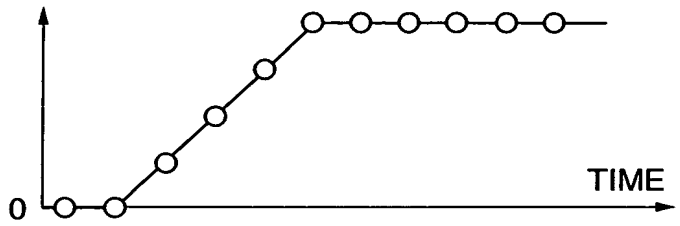

FIG. 2B
Sb

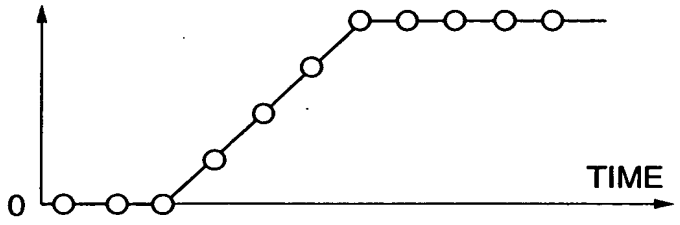

FIG. 2C
Sc

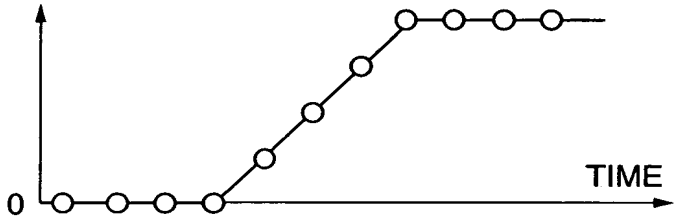

FIG. 2D
Sd

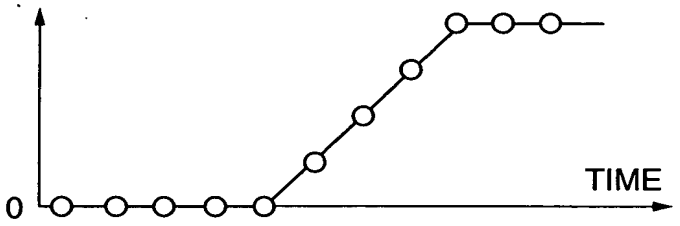

FIG. 2E
Se

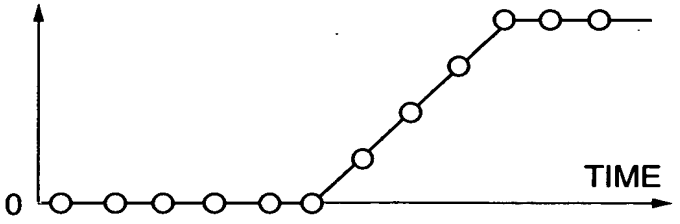

FIG. 2F
Sf

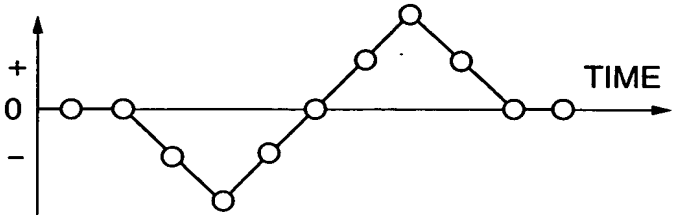

FIG. 3A
Sc

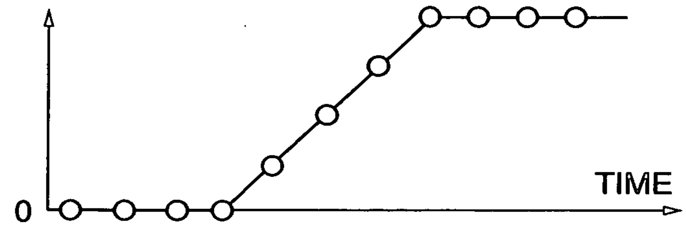

FIG. 3B
Sf

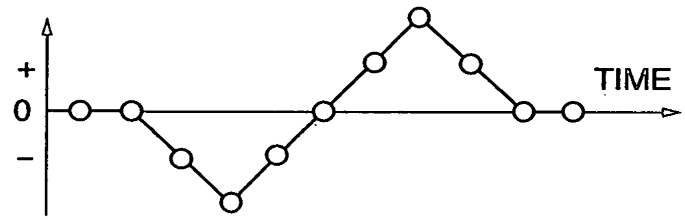

FIG. 3C
Sg

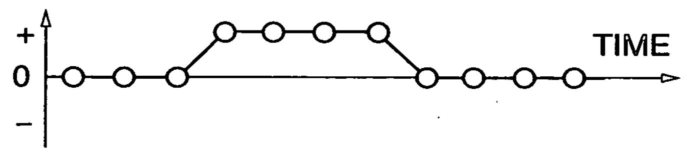

FIG. 3D
Sh

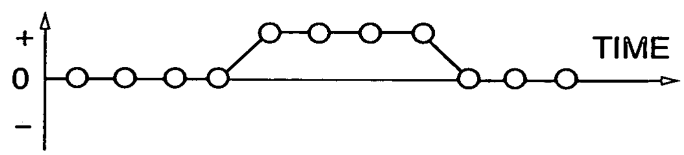

FIG. 3E
Si

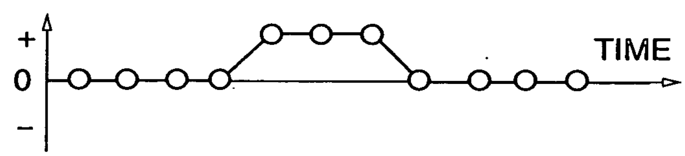

FIG. 3F
Sj

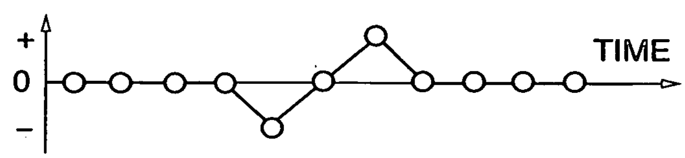

FIG. 3G
Sp

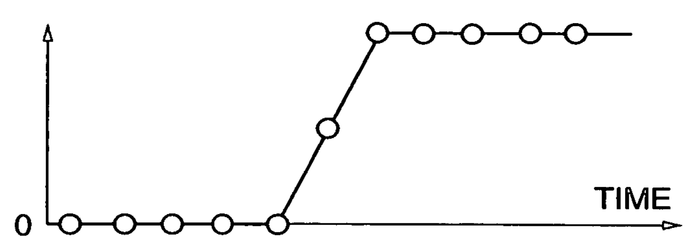

FIG. 4

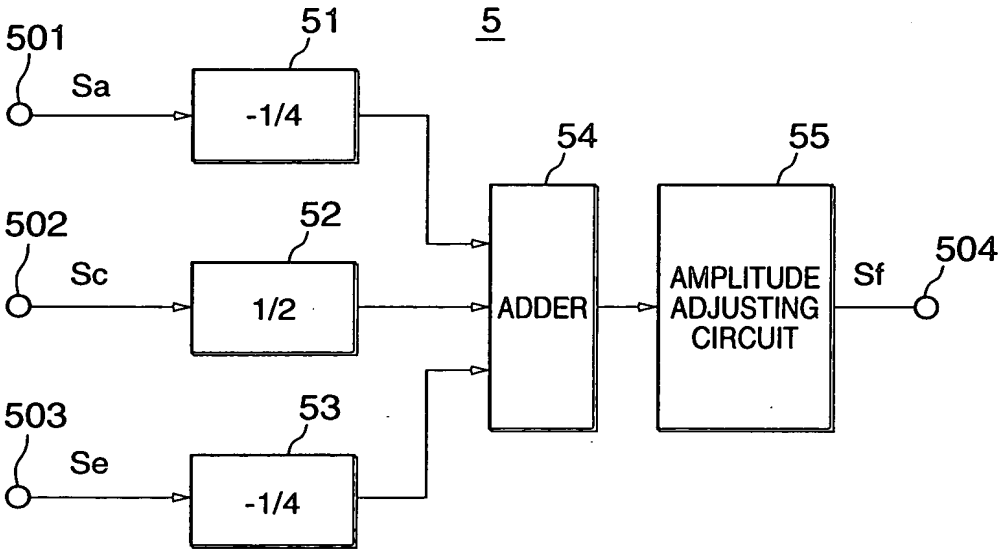
501
Sa
51
-1/4
5
54
55
502
Sc
52
1/2
ADDER
AMPLITUDE ADJUSTING CIRCUIT
Sf
504
503
Se
53
-1/4

FIG. 5

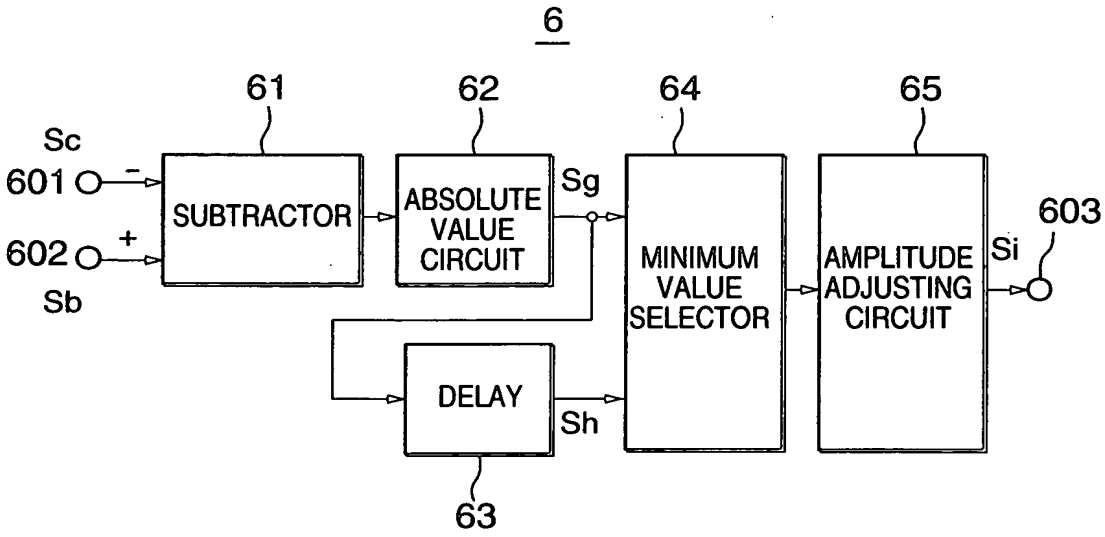
6
61
62
64
65
Sc
601
-
602
+
Sb
SUBTRACTOR
ABSOLUTE VALUE CIRCUIT
Sg
MINIMUM VALUE SELECTOR
AMPLITUDE ADJUSTING CIRCUIT
Si
603
DELAY
Sh
63

FIG. 6

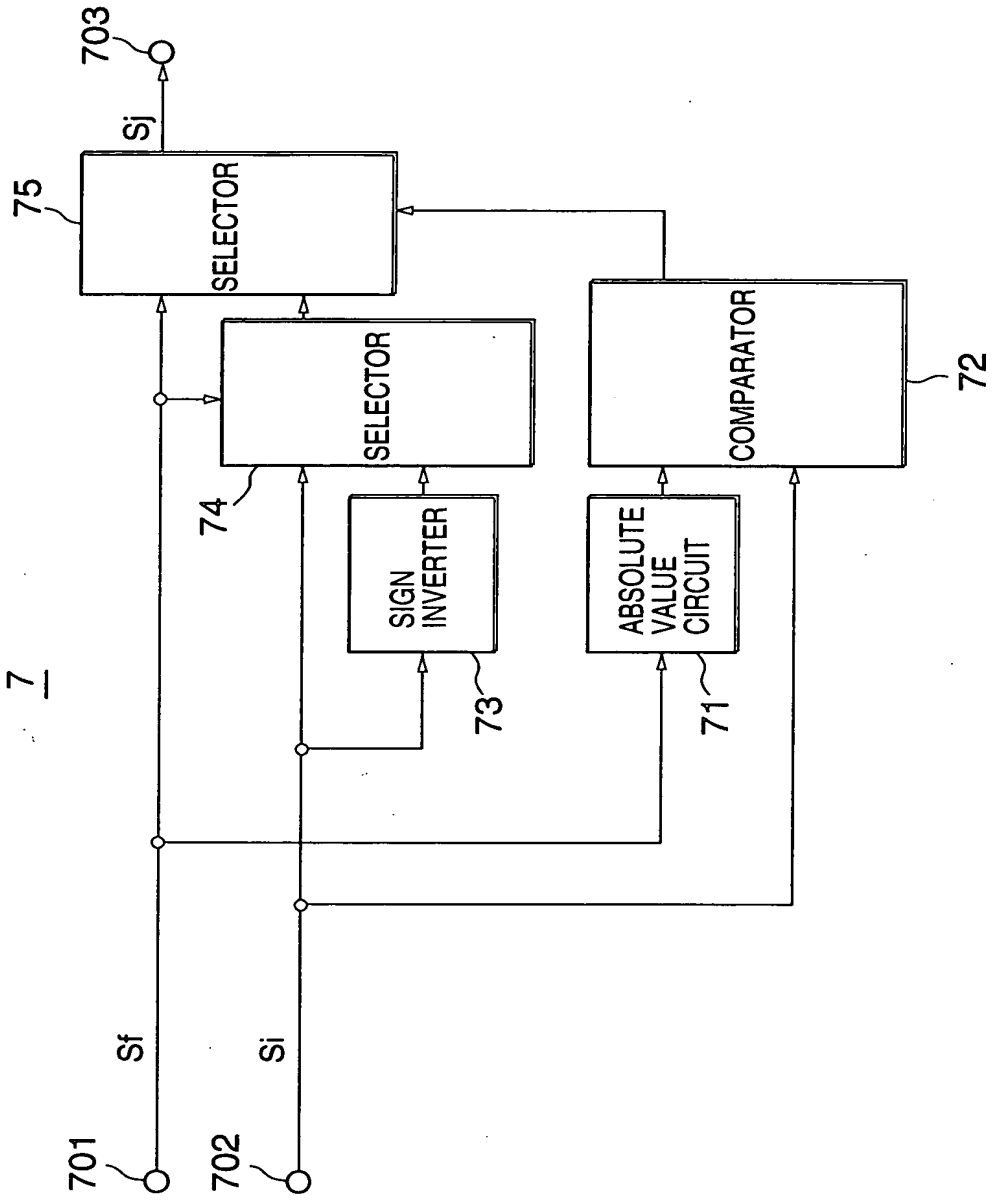
7
701
702
703
Sf
Si
Sj
SELECTOR
75
SELECTOR
74
SIGN INVERTER
73
ABSOLUTE VALUE CIRCUIT
71
COMPARATOR
72

FIG. 7

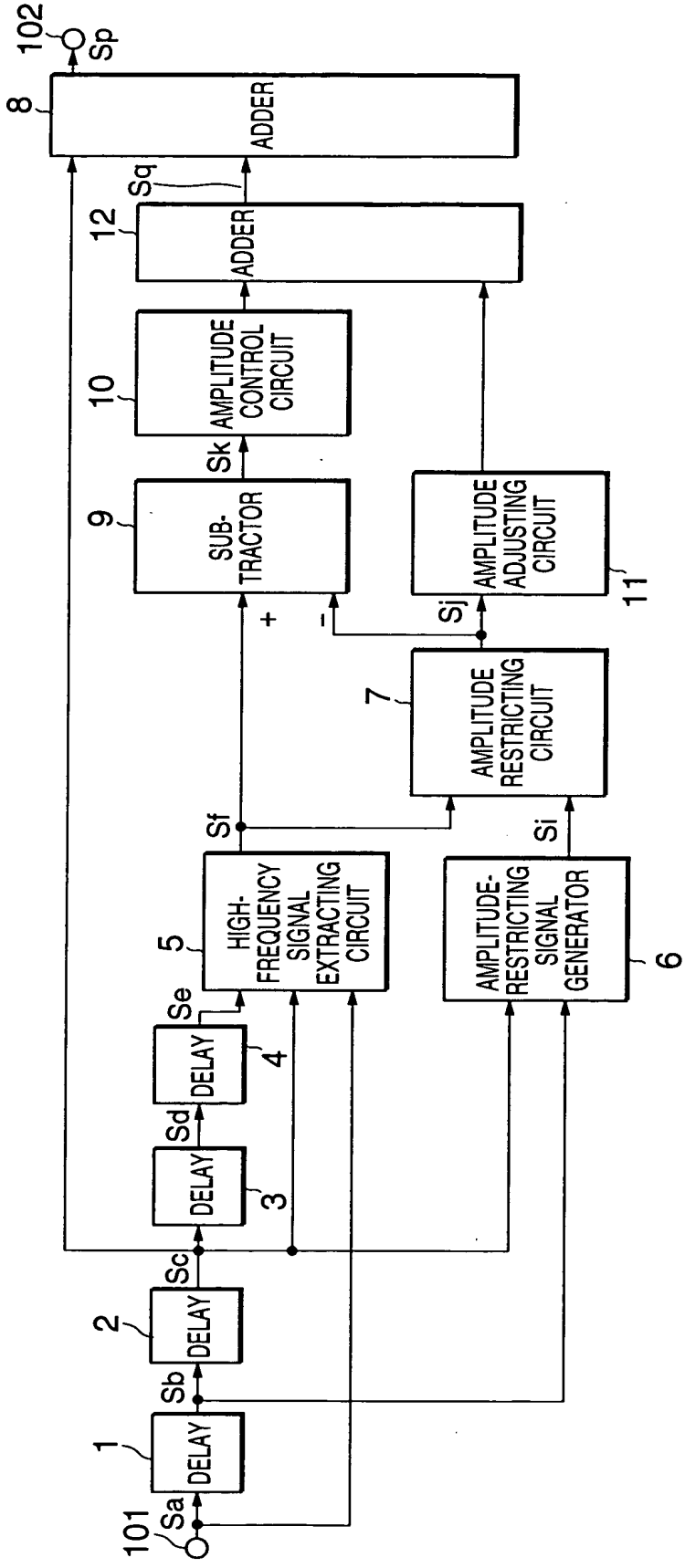
101
Sa
1
DELAY
Sb
2
DELAY
Sc
3
DELAY
Sd
4
DELAY
Se
5
HIGH-FREQUENCY SIGNAL EXTRACTING CIRCUIT
6
AMPLITUDE-RESTRICTING SIGNAL GENERATOR
Si
7
AMPLITUDE RESTRICTING CIRCUIT
Sf
9
SUB-TRACTOR
+
-
Sj
11
AMPLITUDE ADJUSTING CIRCUIT
Sk
10
AMPLITUDE CONTROL CIRCUIT
12
ADDER
Sq
8
ADDER
102
Sp

FIG. 8A

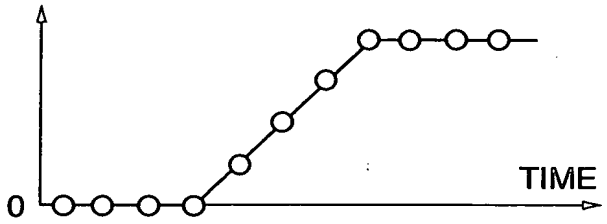

FIG. 8B

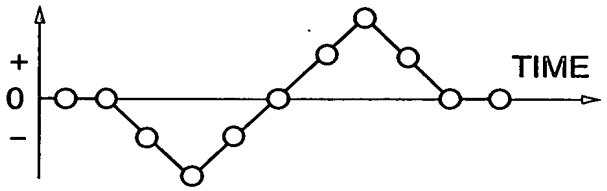

FIG. 8C

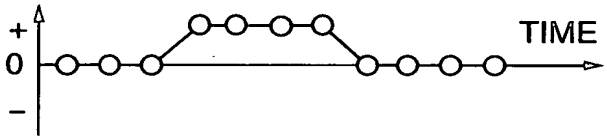

FIG. 8D

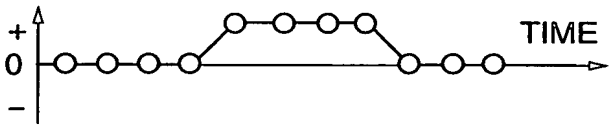

FIG. 8E

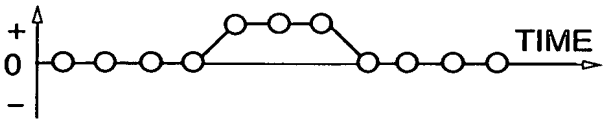

FIG. 8F

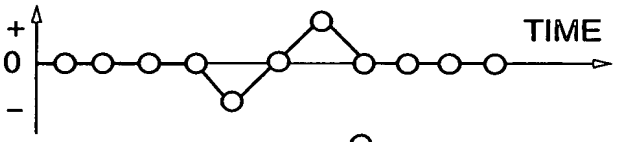

FIG. 8G

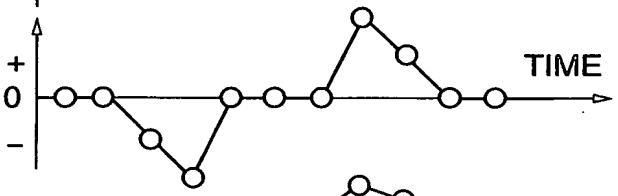

FIG. 8H

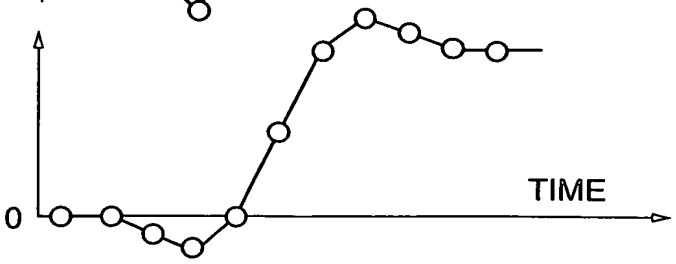

FIG. 9

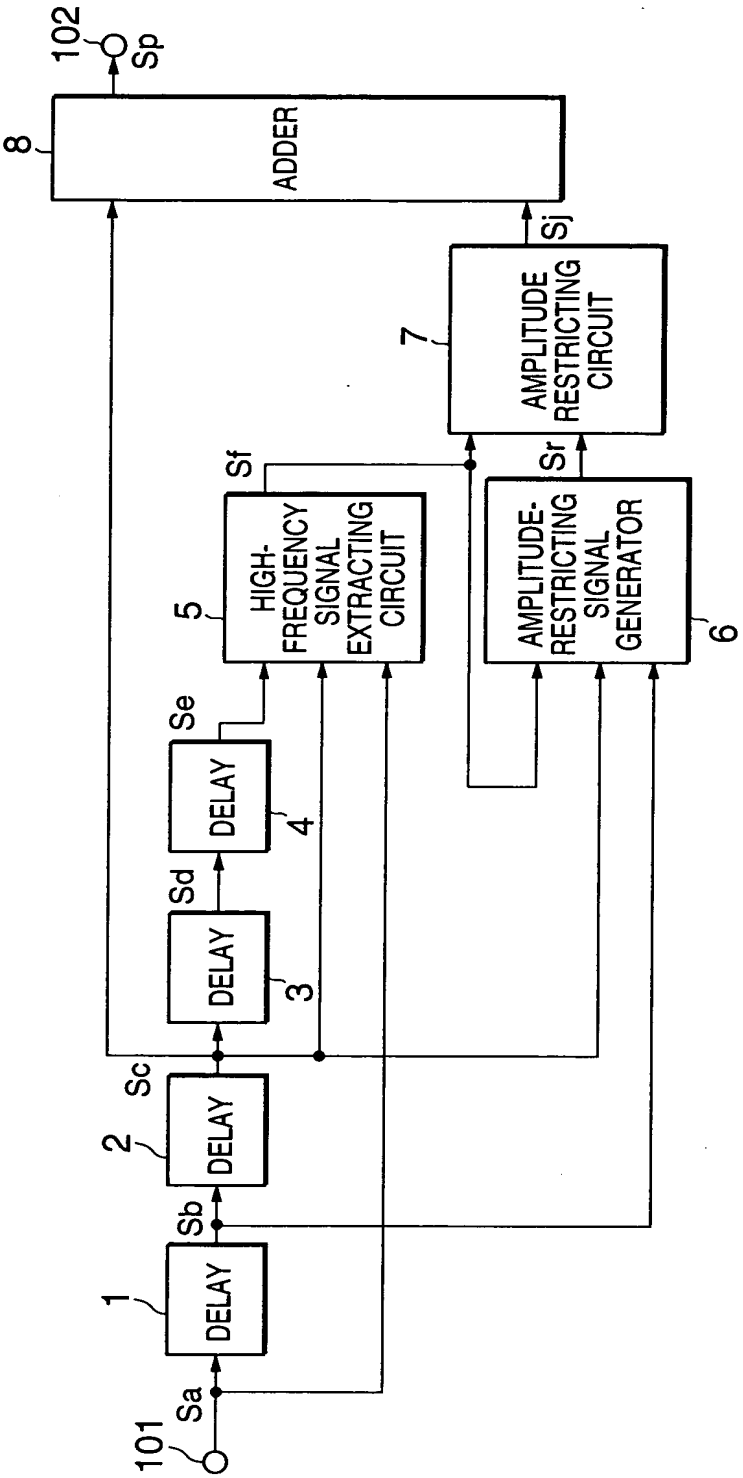
101
Sa
1
DELAY
Sb
2
DELAY
Sc
3
DELAY
Sd
4
DELAY
Se
5
HIGH-FREQUENCY SIGNAL EXTRACTING CIRCUIT
Sf
6
AMPLITUDE-RESTRICTING SIGNAL GENERATOR
Sr
7
AMPLITUDE RESTRICTING CIRCUIT
Sj
8
ADDER
102
Sp

FIG. 10A

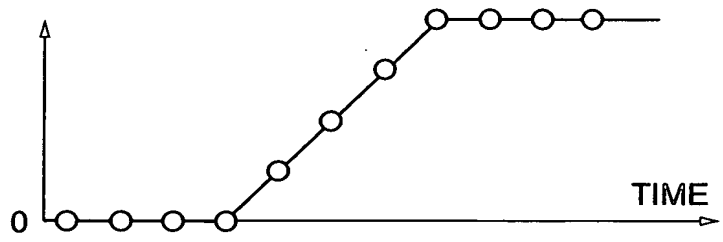

FIG. 10B

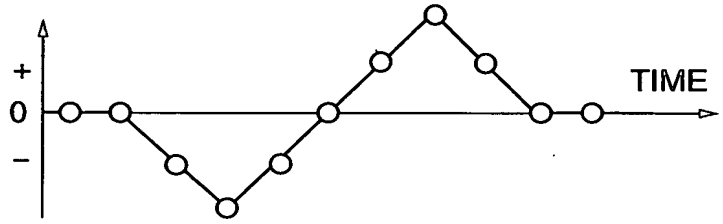

FIG. 10C

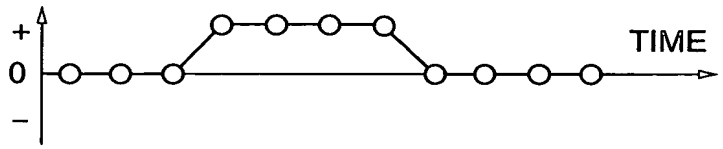

FIG. 10D

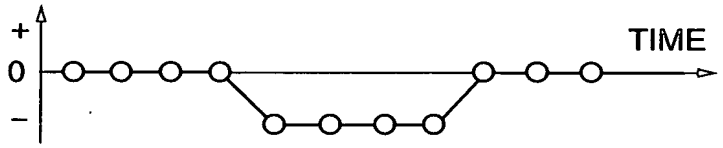

FIG. 10E

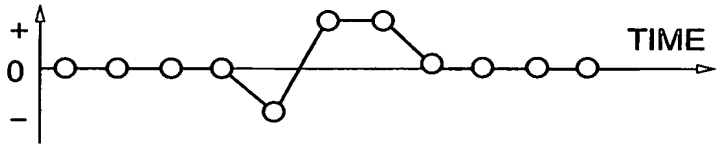

FIG. 10F

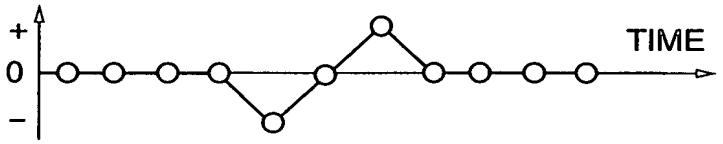

FIG. 10G

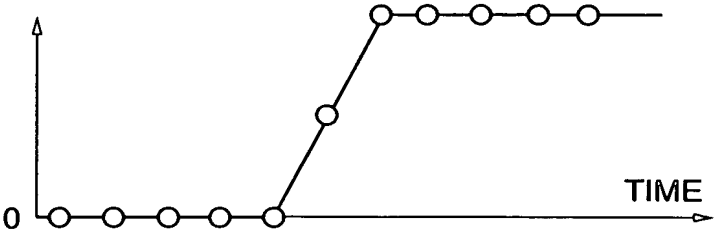

FIG. 11

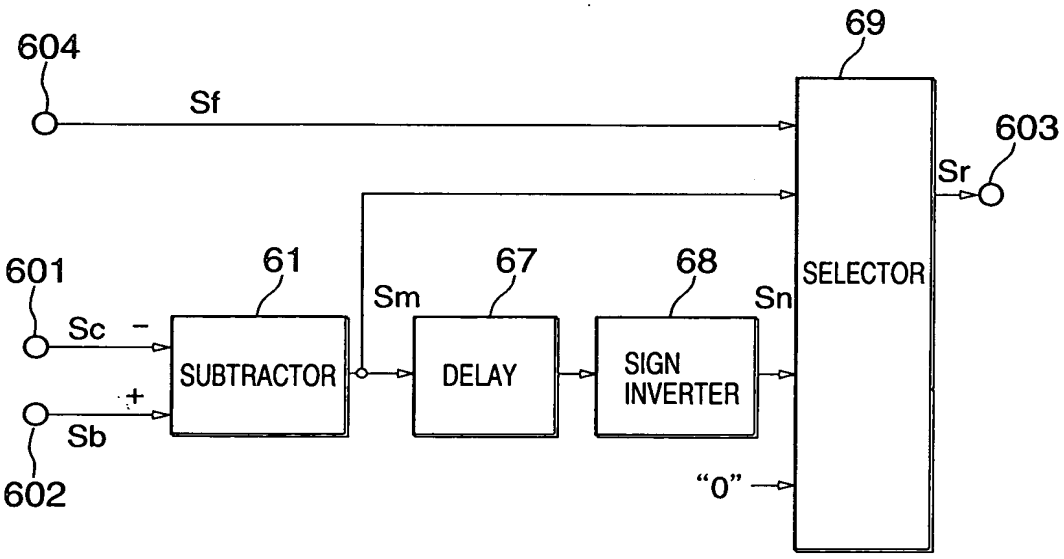
13
604
Sf
69
603
Sr
601
61
67
68
Sm
Sn
SELECTOR
Sc
−
SUBTRACTOR
DELAY
SIGN
INVERTER
+
Sb
602
"0"

FIG. 12

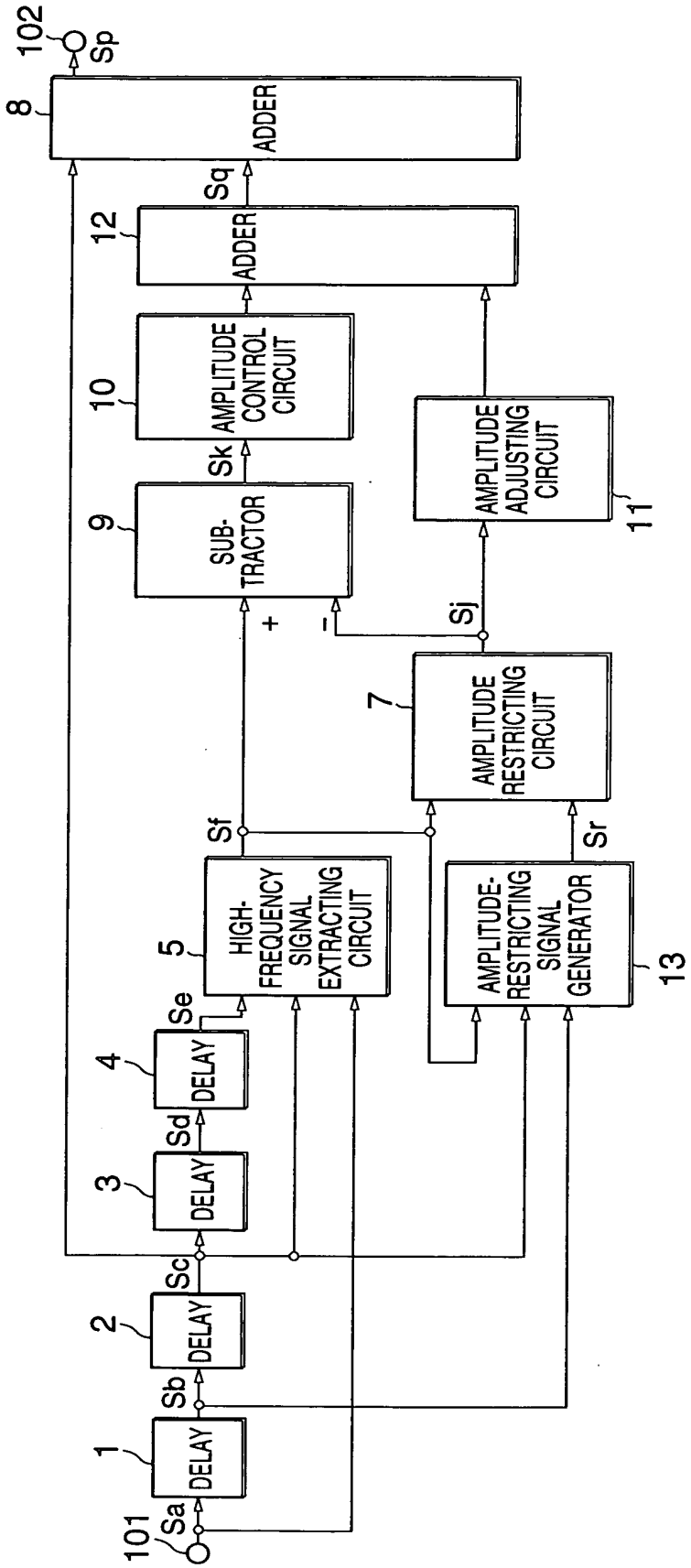
101
Sa
1
DELAY
Sb
2
DELAY
Sc
3
DELAY
Sd
4
DELAY
Se
5
HIGH-FREQUENCY SIGNAL EXTRACTING CIRCUIT
Sf
9
SUB-TRACTOR
+
-
Sk
10
AMPLITUDE CONTROL CIRCUIT
12
ADDER
Sq
8
ADDER
102
Sp
Sj
7
AMPLITUDE RESTRICTING CIRCUIT
11
AMPLITUDE ADJUSTING CIRCUIT
Sr
13
AMPLITUDE-RESTRICTING SIGNAL GENERATOR

FIG. 13

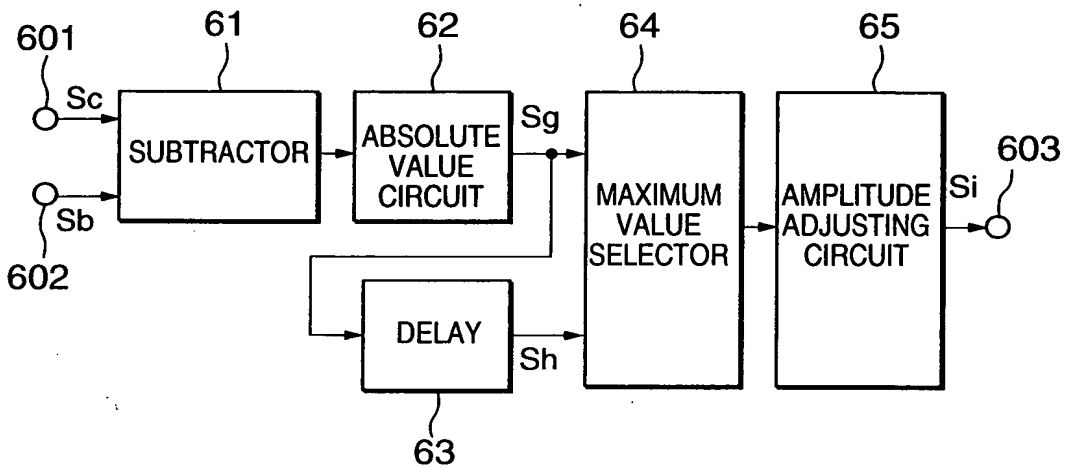
601
61
62
64
65
Sc
SUBTRACTOR
ABSOLUTE VALUE CIRCUIT
Sg
MAXIMUM VALUE SELECTOR
AMPLITUDE ADJUSTING CIRCUIT
Si
603
Sb
602
DELAY
Sh
63

FIG. 14A

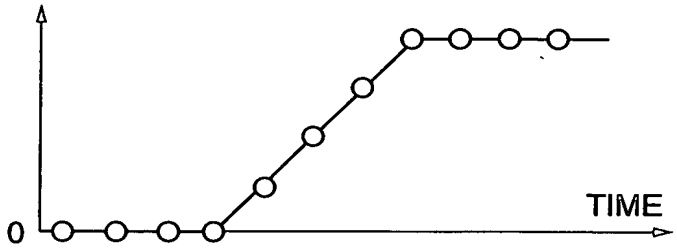

FIG. 14B

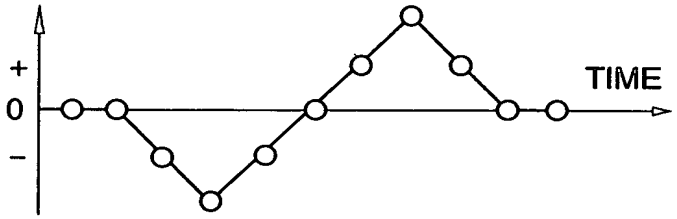

FIG. 14C

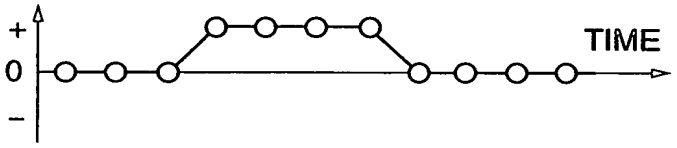

FIG. 14D

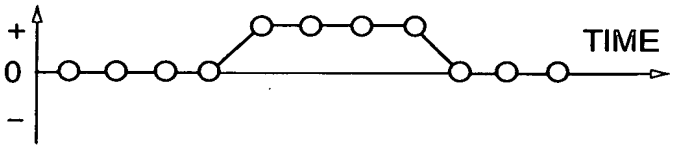

FIG. 14E

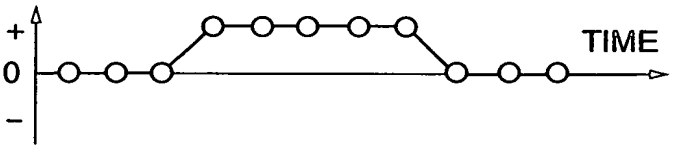

FIG. 14F

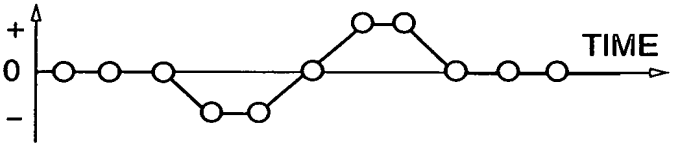

FIG. 14G

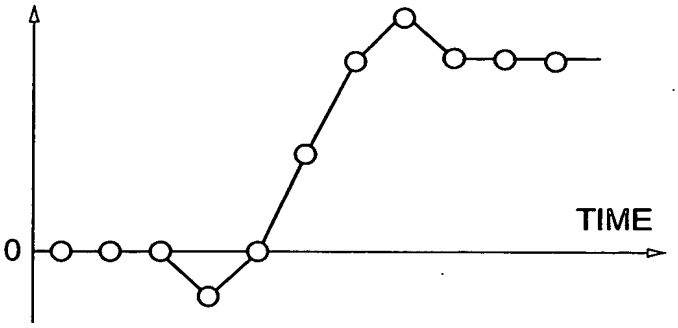

FIG. 15

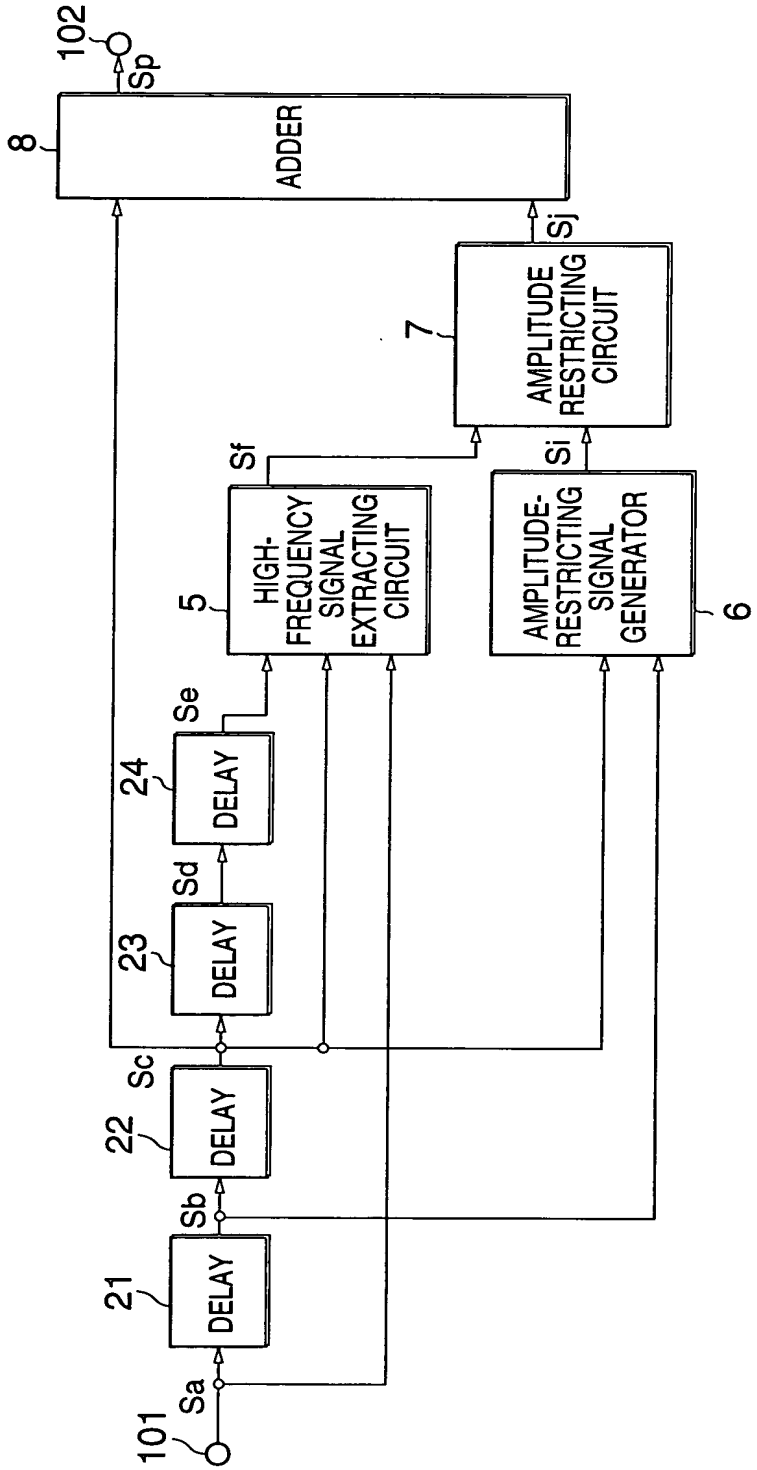
101
Sa
21
DELAY
Sb
22
DELAY
Sc
23
DELAY
Sd
24
DELAY
Se
5
HIGH-FREQUENCY SIGNAL EXTRACTING CIRCUIT
Sf
6
AMPLITUDE-RESTRICTING SIGNAL GENERATOR
Si
7
AMPLITUDE RESTRICTING CIRCUIT
Sj
8
ADDER
102
Sp

FIG. 16

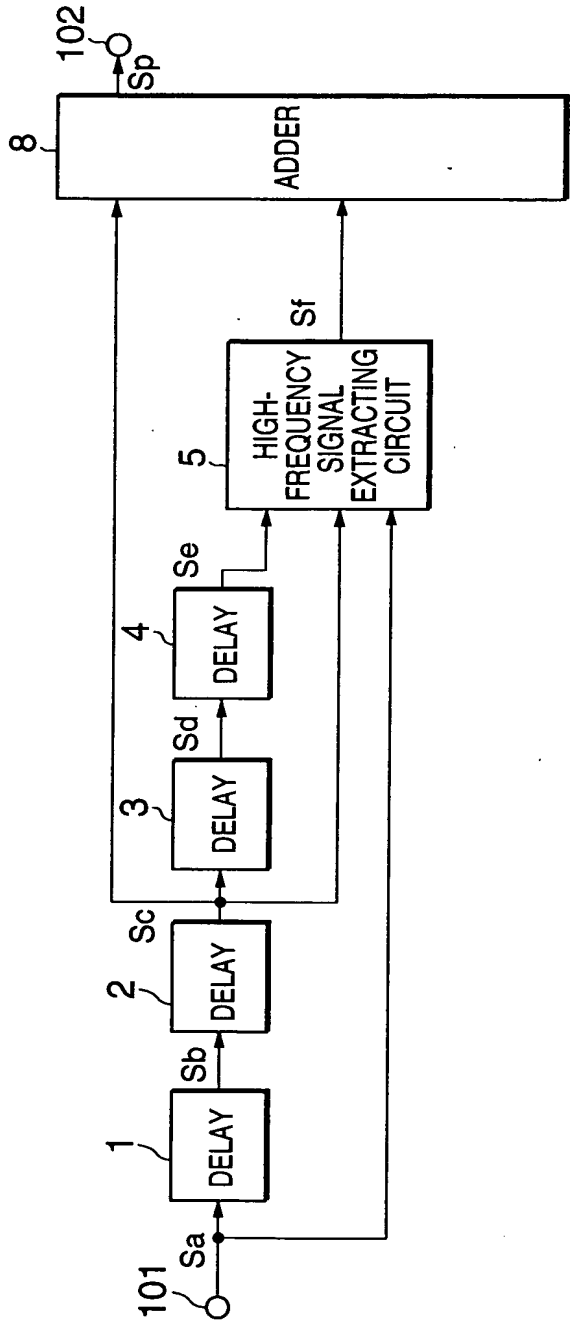
101
Sa
1
DELAY
Sb
2
DELAY
Sc
3
DELAY
Sd
4
DELAY
Se
5
HIGH-FREQUENCY SIGNAL EXTRACTING CIRCUIT
Sf
8
ADDER
102
Sp

FIG. 17A

Sa

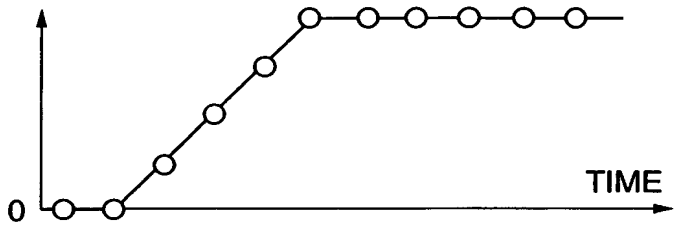

FIG. 17B

Sc

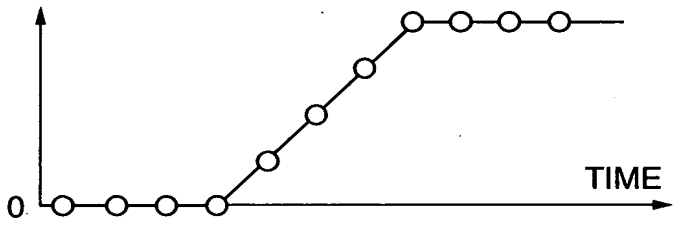

FIG. 17C

Se

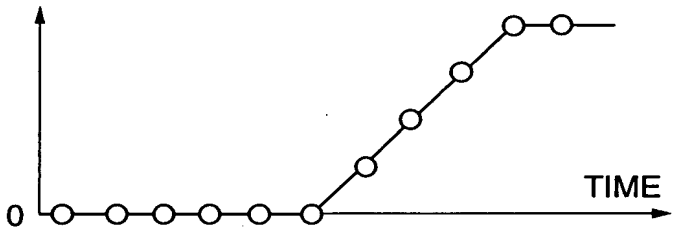

FIG. 17D

Sf

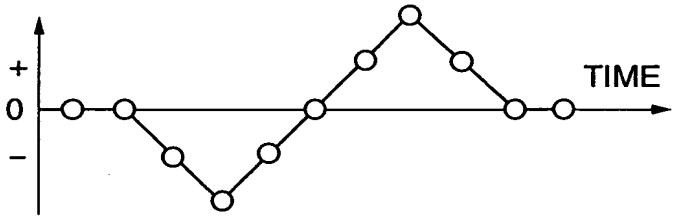

FIG. 17E

Sp